C L A I M S

1. Multiplexer circuit
comprising at least two input channels (IN_0, IN_1) and an output channel (2),
each input channel (IN_0, IN_1) comprising a first transmission gate (FT_0, FT_1) which can be switched on by a select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) for connecting the input channel (IN_0, IN_1) to the output channel (2),
at least one of the input channels (IN_0, IN_1) comprising a bypass circuit (20, 21; 50, 51; 60, 61; 80, 81; 90, 91; 160, 161; 170, 171) for preventing a current flowing through the first transmission gate (FT_0, FT_1) from reaching the other input channel,
and a second transmission gate (ST_0, ST_1), characterized in that a control circuit is provided for controlling said bypass circuit.

2. Multiplexer circuit according to claim 1, wherein said control circuit controls said bypass circuit dependent upon a voltage in the input channel (IN_0; IN_1).

3. Multiplexer circuit according to claim 1, or 2,
wherein said control circuit comprises a sense circuit (120, 130; 121, 131; 140, 150; 141, 151; 100, 110; 101, 111) to control said bypass circuit (80, 90; 81, 91; 160, 161; 170, 171) by sensing a voltage in the input channel (IN_0; IN_1).

4. Multiplexer circuit according to one of claims 1 to 3,
wherein each input channel (IN_0, IN_1) comprises a bypass circuit (20, 21; 50, 51; 60, 61; 80, 81; 90, 91; 160, 161; 170, 171) and a second transmission gate (ST_0, ST_1).

5. Multiplexer circuit according to claim 4, wherein the bypass circuit (20, 21; 50, 51; 60, 61) is switched on for an

input channel (IN_0) which is not selected and is switched off for a selected input channel (IN_1).

6. Multiplexer circuit according to one of claims 1 to 5, wherein said bypass circuit comprises a pull-down circuit (20, 21; 50, 51; 80, 81; 160, 161) reducing an input voltage for the second transmission gate (ST_0, ST_1).

7. Multiplexer circuit according to one of claims 1 to 6, wherein said bypass circuit (20, 21) is controlled by said select signal ($\overline{SELECT_0}$, $\overline{SELECT_1}$).

8. Multiplexer circuit according to one of claims 1 to 7, wherein said bypass circuit (20, 21; 50, 51) is an NMOS transistor the gate of which is controlled by said select signal ($\overline{SELECT_0}$, $\overline{SELECT_1}$), the drain of which is connected with an output of said first transmission gate (FT_0, FT_1) and the source of which is connected with ground potential (V_{SS}).

9. Multiplexer circuit according to one of claims 1 to 8, wherein said bypass circuit comprises a pull-up circuit (60, 61; 90, 91; 170, 171) increasing an input voltage for said second transmission gate (ST_0, ST_1).

10. Multiplexer circuit according to claim 9, wherein said pull-up circuit (60, 61; 90, 91; 170, 171) is a PMOS transistor the drain of which is connected with an output of said first transmission gate (FT_0, FT_1) and the source of which is connected with a power supply voltage level (V_{CC}).

11. Multiplexer circuit according to claims 1 to 10, wherein said control circuit controls said bypass circuit by means of said select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) and an input voltage (U_1, U_2) applied to said input channel (IN_0, IN_1).

12. Multiplexer circuit according to claims 8 to 11, wherein said control circuit controls said pull-up circuit (60, 61) and said pull-down circuit (50, 51) by means of said select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) and an input voltage (U_1, U_2) applied to said input channel (IN_0, IN_1).

13. Multiplexer circuit according to claim 12, wherein said control circuit comprises a NAND gate (110, 111) the output of which is connected with the gate of said PMOS transistor (90, 91) and a NOR gate (100, 101) the output of which is connected with the gate of said NMOS transistor (80, 81).

14. Multiplexer circuit according to claim 13, wherein said NAND gate receives the input voltage and the inverted select signal ($\overline{SELECT_0}$, $\overline{SELECT_1}$) and said NOR gate receives the input voltage and the select signal ($SELECT_0$, $SELECT_1$).

15. Multiplexer circuit according to one of claims 2 to 10, wherein said sense circuit (120, 130; 121, 131; 140, 150; 141 151) is formed so as to sense a voltage in the input channel (IN_0, IN_1) at the input of said first transmission gate (FT_0, FT_1)or between said first transmission gate (FT_0, FT_1) and said second transmission gate (ST_0, ST_1).

16. Multiplexer circuit according to claim 15, wherein a pull-down bypass circuit is formed of a NMOS transistor (160; 161) the drain of which is connected with an output (70, 71) of said first transmission gate (FT_0, FT_1) and the source of which is connected with the ground level (V_{SS}) and wherein said sense circuit is formed of a PMOS transistor (130; 131) and an NMOS transistor (120; 121) in series the source of the NMOS transistor (120; 121) being connected to ground level (V_{SS}) and the source of PMOS transistor (130; 131) being connected to an output (70, 71) of said first transmission gate (FT0, FT1) and wherein the drains of said PMOS transistor (130; 131) and said NMOS transistor (120; 121) are connected

to each other and to the gate of the NMOS bypass transistor (160; 161).

17. Multiplexer circuit according to claim 15 or 16, wherein said pull up bypass circuit is formed of a PMOS transistor (170; 171) the drain of which is connected with an output (70; 71) of said first transmission gate (FT_0, FT_1) and the source of which is connected with power supply voltage level (V_{CC}) and wherein said sense circuit is formed of a PMOS transistor (150; 151) and an NMOS transistor (140; 141) in series the source of the PMOS transistor (150; 151) being connected to power supply voltage level (V_{CC}) and the source of the NMOS transistor (140; 141) being connected to an output (70; 71) of said first transmission gate (FT_0, FT_1) and wherein the drains of the PMOS transistor (150; 151) and the NMOS transistor (140; 141) are connected to each other and to the gate of the PMOS bypass transistor (170, 171).

18. Analogue-to-digital converter comprising a multiplexer circuit according to one of claims 1 to 17.